DESIGN AND PERFORMANCE ANALYSIS OF A NINE-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER WITH INTELLIGENT FAULT DIAGNOSIS AND ACTIVE FAULT-TOLERANT CONTROL

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Abstract - Semiconductor switching faults can disrupt voltage synthesis in cascaded H-bridge multilevel inverters, causing waveform distortion and reduced output capability. This paper presents an active fault-management framework for a nine-level cascaded H-bridge inverter that coordinates phase-disposition pulse-width modulation, fault detection and isolation, and redundant switching. The study focuses on extending coordinated diagnostic and recovery operation to a nine-level configuration, with particular attention to the relationship between fault identification, switching-path replacement, and retained output-voltage capability. A MATLAB/Simulink model integrates the inverter, modulation subsystem, controlled fault injection, and supervisory control. Healthy operation, uncompensated fault operation, and fault-tolerant operation form the comparative assessment framework. Output voltage, load current, harmonic distortion, and recovery behaviour provide the principal performance measures. The intended contribution is the coordinated evaluation of diagnosis and reconfiguration within the nine-level architecture, including the distinction between continued operation and complete restoration of the available voltage levels. The framework provides a basis for determining the operating limits of redundant-path recovery; quantitative validation and hardware testing remain necessary to establish improvements in power quality, recovery speed, and reliability.

Index Terms— Active fault-tolerant control, cascaded H-bridge inverter, fault detection and isolation, nine-level inverter, phase-disposition pulse-width modulation, redundant switching, total harmonic distortion.

I. INTRODUCTION

Reliable power conversion is essential to the effective operation of renewable energy systems, industrial drives, and other applications that require a continuous electrical supply. In these systems, inverter performance depends on both the quality of the output waveform and the ability to withstand component failures. Multilevel inverters offer an attractive approach to medium- and high-voltage conversion by synthesising an alternating output from several discrete voltage levels. This stepped waveform can reduce harmonic distortion and voltage stress compared with a conventional two-level inverter under comparable operating conditions. However, the increased number of semiconductor devices and associated gate-driving circuits creates additional opportunities for faults, making fault management an important consideration in converter design.

Among multilevel inverter configurations, the cascaded H-bridge (CHB) topology provides a modular structure in which individual converter cells contribute to the total output voltage. Its modularity facilitates voltage scaling and independent control of the constituent cells. A symmetrical nine-level CHB inverter typically combines four H-bridge cells supplied by equal isolated DC sources to generate nine output-voltage levels. Although this arrangement offers flexibility in waveform synthesis, its performance depends on the correct operation of the switches within each cell. A failure in one device can alter the available switching states, distort the output waveform, and reduce the converter's ability to deliver the required voltage and power.

Power semiconductor faults present different challenges according to their nature and location. An open-switch fault can prevent a required conduction path from being established, producing missing voltage levels, waveform asymmetry, and increased harmonic distortion. A short-circuit fault can cause excessive current and requires rapid protection and electrical isolation before continued operation can be considered. Consequently, an effective fault-management strategy must establish which faults can be accommodated and which require protective shutdown. Fault detection alone is insufficient to maintain service; the diagnostic decision must be linked to an appropriate isolation and recovery mechanism.

Fault-tolerant control provides a means of sustaining converter operation when a recoverable fault occurs. Passive approaches use a predetermined control structure designed to accommodate a defined range of abnormalities. Active approaches incorporate a diagnostic stage that detects a fault, identifies the affected component or converter cell, and initiates a suitable control or circuit reconfiguration. In a CHB inverter, recovery may involve bypassing a damaged cell, modifying the modulation strategy, or activating a redundant switching path. Each option involves trade-offs

among hardware requirements, achievable output voltage, diagnostic complexity, and post-fault waveform quality.

The diagnostic stage must distinguish faults from normal changes in operating conditions. Load variations, DC-source fluctuations, and modulation changes can affect voltage and current measurements even when the inverter is healthy. Indicators such as output-voltage deviation, waveform asymmetry, and harmonic content can support fault assessment, but their effectiveness depends on the measurement window and decision logic. In particular, detecting an abnormal output does not necessarily identify the failed switch. A practical fault detection and isolation unit therefore requires a clear relationship between the monitored signals, expected switching behaviour, and the fault location.

Modulation also plays an important role in coordinating normal and post-fault operation. Phase-disposition pulse-width modulation (PD-PWM) uses vertically displaced carriers with a common phase relationship to generate the required voltage levels. Its structured carrier arrangement provides a suitable basis for implementing multilevel switching commands and integrating supervisory fault-management logic. Following fault isolation, the gating commands must be transferred to an available recovery path in a controlled manner. The success of this transition should be assessed through the restoration of the output waveform, recovery time, voltage deviation, and harmonic performance.

This study investigates an active fault-tolerant control arrangement for a nine-level cascaded H-bridge multilevel inverter using PD-PWM, a fault detection and isolation unit, and redundant switching. The objective is to coordinate fault identification and corrective switching so that the inverter can continue operating under the fault conditions supported by its recovery architecture. A MATLAB/Simulink model is used to examine healthy operation, faulty operation without compensation, and operation with the fault-tolerant controller enabled. The comparative assessment focuses on output-voltage and load-current behaviour, waveform distortion, and the transition following fault occurrence. Through this analysis, the study evaluates the effectiveness and limitations of the integrated diagnostic and recovery arrangement in supporting continuity of inverter operation.

II. LITERATURE REVIEW

2.1 Fault Diagnosis in Cascaded H-Bridge Multilevel Inverters

Fault diagnosis in cascaded H-bridge (CHB) multilevel inverters involves detecting abnormal operation and identifying the affected switch or converter cell. Because the output waveform is produced by several independently controlled cells, a semiconductor fault can alter the available voltage levels and introduce characteristic waveform distortion. These changes provide useful diagnostic information, although reliable identification requires distinguishing fault effects from normal operating transients.

Lezana, Aguilera, and Rodríguez (2009) proposed a fault-detection method based on output-voltage frequency analysis. Their approach used one voltage measurement per output phase and analysed high-frequency harmonic behaviour to identify faulty cells. Dynamic prediction helped prevent incorrect detection during normal transients. Experimental results supported the method's ability to detect faulty cells, which could subsequently be bypassed to permit continued operation. This study established output-voltage analysis as a useful foundation for diagnosing faults with limited sensing requirements.

2.2 Diagnosis Using Harmonic Distortion and Normalised Voltage

Harmonic distortion and normalised voltage indicators provide relatively simple ways to assess changes in inverter operation. Harmonic content describes waveform deformation, while a normalised voltage factor can reveal changes in output magnitude or symmetry. Their combined use can provide more diagnostic information than either indicator alone.

Mehta, Sahoo, and Kumar (2021) investigated fault diagnosis in a five-level CHB inverter using total harmonic distortion and a normalised output-voltage factor. The study employed level-shifted pulse-width modulation and examined healthy and faulty operating conditions. Simulation and hardware tests at different power factors supported the proposed approach. A post-fault strategy based on reduced amplitude modulation enabled continued operation, although this involved a compromise in output-voltage capability. The work demonstrates the value of simple diagnostic features while highlighting the importance of assessing retained performance after fault isolation.

2.3 Active Fault-Tolerant Control with Redundant Switching

Active fault-tolerant control combines diagnostic decisions with corrective action. After a fault is detected and localised, the controller modifies the switching arrangement or activates a redundant conduction path. The effectiveness of this approach depends on accurate diagnosis, successful electrical isolation, and coordinated transfer of gating commands.

Alqarni (2022) presented a seven-level fault-tolerant CHB inverter incorporating a fault detection and isolation unit, standby redundant switching, and phase-disposition pulse-width modulation. Total harmonic distortion and a

normalised output-voltage factor were employed for fault diagnosis. The architecture was evaluated in MATLAB/Simulink, and Markov-chain analysis was used to investigate reliability.

This study provides a particularly close reference for the present investigation because it combines the principal elements described in the proposed nine-level system. Consequently, a contribution must be demonstrated through a specific extension, such as improved fault discrimination, broader operating-condition coverage, or better recovery performance. Increasing the number of output levels alone does not establish an improved fault-management method.

2.4 Fuzzy-Logic-Based Fault Identification

Fuzzy logic offers a structured means of converting measured waveform features into diagnostic decisions. It can represent relationships between operating indicators and fault locations through membership functions and inference rules.

Mehta, Sahoo, and Dhiman (2022) proposed a fuzzy-logic method for identifying open-circuit switch faults in a five-level CHB inverter. Output-voltage total harmonic distortion and normalised average output voltage were used as input variables. The fuzzy controller classified the faulty switch, while a reduced modulation index supported balanced post-fault operation. MATLAB/Simulink and prototype results were presented to validate the method.

The study illustrates the importance of explicitly connecting diagnostic features to individual switch faults. For the present system, the detection and isolation logic should similarly explain how the selected measurements distinguish fault locations, including cases that produce comparable output distortion.

2.5 Automated Fault Detection and Inverter Reconfiguration

Recent investigations have increasingly treated fault detection and circuit reconfiguration as a coordinated process. This approach evaluates both the identification of a fault and the ability of the remaining circuit to recover useful operating characteristics.

Singh, Yadav, and Gupta (2025) developed an automated fault-detection and reconfiguration method for a five-level hybrid multilevel inverter. The topology combined a main conversion unit with a redundant H-bridge. Output-voltage measurements and discrete Fourier processing supported fault detection, after which a reconfiguration scheme restored the required switching operation. The investigation considered open- and short-circuit faults, multiple switch failures, and variations in load, source conditions, and modulation index. Simulation and experimental assessments supported the proposed arrangement.

Although the hybrid topology differs from a conventional CHB inverter, this study provides relevant evaluation criteria. These include fault coverage, redundant hardware requirements, retained voltage levels, and performance under changing operating conditions.

2.6 Research Gap and Scope of the Present Study

The reviewed literature establishes waveform-based diagnosis, modulation adjustment, and redundant switching as recognised approaches to multilevel inverter fault management. The remaining task for the present study is to demonstrate how its particular nine-level CHB architecture performs under clearly defined faults and operating conditions.

The investigation therefore focuses on coordinating phase-disposition PWM, fault detection and isolation, and redundant switching within a nine-level CHB inverter. Healthy operation, uncompensated fault operation, and compensated operation should be compared using output-voltage and load-current waveforms, harmonic distortion, detection delay, and recovery time. The assessment should also establish which voltage levels and output capabilities are retained after corrective switching.

The contribution should be defined by these demonstrated results and by comparison with closely related architectures. Claims of improved reliability, faster recovery, or superior waveform quality require corresponding quantitative evidence.

III. PROBLEM STATEMENT

A nine-level cascaded H-bridge multilevel inverter depends on coordinated semiconductor switching to generate the required stepped output voltage. A switch fault can interrupt a conduction path, eliminate voltage levels, and introduce waveform asymmetry and harmonic distortion. These disturbances can reduce power delivery, increase electrical stress, and interrupt inverter operation. An effective fault-management arrangement must therefore identify the affected device and initiate an appropriate corrective response.

The principal challenge is to detect and localise a switch fault while distinguishing its effects from normal variations in load, DC-source voltage, and modulation conditions. Total harmonic distortion can indicate waveform deterioration, but it does not independently establish the fault location. A normalised output-voltage indicator can provide additional information, although its relationship with individual switch faults must be defined through explicit diagnostic rules. Reliable diagnosis is essential because an incorrect decision can activate an unsuitable recovery path, while delayed detection can prolong degraded operation.

Post-fault recovery also depends on the available redundancy and the coordination of switching commands. The faulty conduction path must be isolated before its function is transferred to a standby device. This transition should preserve acceptable output characteristics without introducing conflicting switching states or excessive disturbances. Continued operation must consequently be evaluated through retained voltage levels, output magnitude, load-current behaviour, recovery time, and harmonic distortion.

Accordingly, this study aims to develop and evaluate an integrated fault detection, isolation, and tolerant-control arrangement for a nine-level cascaded H-bridge inverter using MATLAB/Simulink. The proposed arrangement combines phase-disposition pulse-width modulation, diagnostic indicators based on harmonic distortion and normalised output voltage, and redundant switching for explicitly defined recoverable faults. The investigation compares healthy operation, faulty operation without compensation, and operation with fault-tolerant control enabled. It also examines selected load and modulation changes to assess diagnostic robustness. The objective is to establish the fault conditions under which the arrangement can sustain inverter operation and quantify its recovery performance and limitations.

IV. MATHEMATICAL MODELLING

The mathematical model describes the voltage synthesis, load dynamics, fault diagnosis, and recovery operation of the nine-level cascaded H-bridge inverter. A symmetrical configuration is considered, comprising four series-connected H-bridge cells supplied by equal isolated DC sources. The model initially assumes ideal switches and constant DC-source voltages; practical switching losses, dead time, and source variations can subsequently be incorporated into the simulation.

4.1 Nine-Level Inverter Model

Each H-bridge cell generates a positive, zero, or negative voltage according to its switching state. The total inverter output is the sum of the four cell voltages:

$$v_o(t) = \sum_{k-1}^{4} s_k(t) V_{dc,k}, \qquad s_k(t) \in \{-1, 0, +1\} \qquad (1)$$

Here, v_o is the inverter output voltage, $V_{dc,k}$ is the DC voltage of cell k, and s_k represents its effective switching state. For equal DC-source voltages, the available output levels are:

$$v_o \in \{-4V_{dc}, -3V_{dc}, -2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}\} \qquad (2)$$

These nine voltage levels form the stepped waveform used to approximate the sinusoidal reference. Equation (2) describes healthy operation; the levels available after a fault depend on the affected device and the recovery circuit.

4.2 Phase-Disposition PWM Model

Phase-disposition PWM uses eight vertically displaced triangular carriers with a common phase and frequency. A sinusoidal reference is compared with these carriers to determine the requested output level. For carriers normalised to span the interval from -1 to +1, the reference is:

$$r(t) = m_a \sin(2\pi f_1 t), \qquad 0 \le m_a \le 1 \qquad (3)$$

where m_a is the amplitude modulation index and f_1 is the fundamental output frequency. The requested voltage-level index is obtained from:

$$\ell^*(t) = \sum_{j=1}^{8} \mathbf{1}[r(t) \ge c_j(t)] - 4 \qquad (4)$$

In Equation (4), c_j is the jth carrier and 1[.] equals one when the comparison is true and zero otherwise. The resulting index ranges from -4 to +4. A switching-state allocation table converts this index into individual H-bridge gating commands while preventing simultaneous conduction of complementary switches. The same allocation stage must account for the switching paths available after a fault.

4.3 Load Dynamics

For a series resistive–inductive load, the relationship between inverter output voltage and load current is:

$$L\frac{di_o(t)}{dt} + Ri_o(t) = v_o(t) \qquad (5)$$

where R and L denote load resistance and inductance, respectively, and i_o is the load current. This model captures current continuity and the transient response following fault occurrence or switching reconfiguration. A resistive load is represented by setting L=0.

4.4 Fault Representation and Diagnostic Indicators

A switch fault changes the voltage that a cell can produce for a given gating command. Its effect can be represented at the inverter output as:

$$v_o^f(t) = \sum_{k=1}^{4} [s_k^*(t) V_{dc,k} + \Delta v_{f,k}(t)] \qquad (6)$$

Here, s_k^* is the commanded healthy switching state and $\Delta v_{f,k}$ is the voltage deviation caused by the fault in cell k. For an unaffected cell, this deviation is zero. For a faulty cell, it depends on the failed switch, current direction, diode conduction, and commanded state. An open-switch fault should therefore be implemented at device level rather than represented by simply setting the entire cell voltage to zero.

Two waveform indicators are considered for diagnosis. Output-voltage total harmonic distortion is calculated as:

$$\mathrm{THD}_v = \frac{\sqrt{\sum_{h=2}^{H} V_{h,\mathrm{rms}}^2}}{V_{1,\mathrm{rms}}} \times 100\% \qquad (7)$$

where $V_{1,rms}$ is the fundamental RMS voltage and $V_{h,rms}$ is the RMS voltage of harmonic order h. The harmonic limit H and analysis window must remain consistent across the compared operating conditions.

For this formulation, a signed normalised average output voltage is defined as:

$$\eta_v(t) = \frac{1}{4V_{dc}T_w}\int_{t-T_w}^{t} v_o^f(\tau)\,d\tau \qquad (8)$$

where T_w is an integer number of fundamental periods. Under balanced, steady-state operation, this indicator is approximately zero. A nonzero value can reveal waveform asymmetry, although some faults may produce little change in the average. Consequently, neither this indicator nor THD alone guarantees unique switch identification.

The diagnostic input is the pair $\{THD_v, \eta_v\}$ Fault-specific decision regions must be established from device-level fault simulations over the intended operating range. A fault is assigned to a particular switch only when its diagnostic region is distinguishable from healthy operation and other fault cases. Where these regions overlap, additional information, such as cell voltage or current polarity, is required.

4.5 Fault-Tolerant Recovery and Performance Measures

After diagnosis, the controller isolates the faulty path and transfers its switching function to an available redundant path. The post-fault inverter voltage is:

$$v_o^{FTC}(t) = \sum_{k=1}^{4} \tilde{v}_k(t) \qquad (9)$$

where $v_k^{\sim}$ is the actual cell voltage after reconfiguration. Full restoration of the nine voltage levels is possible only when the redundant circuit reproduces the required healthy cell states. Otherwise, the model must represent the resulting reduction in voltage capability.

Detection and recovery performance are quantified by:

$$t_d = t_{\text{det}} - t_f, \qquad t_r = t_{\text{rec}} - t_f \qquad (10)$$

Here, t_f is the fault-injection instant, t_{det} is the detection instant, and t_{rec} is the instant at which the output returns to a predefined tolerance band and remains within it for a specified settling interval. Recovery is assessed alongside THD, waveform symmetry, and retained fundamental voltage. Together, these measures establish whether the control arrangement restores the intended operating condition or sustains operation at a reduced capability.

V. MODEL IMPLEMENTATION

The nine-level cascaded H-bridge multilevel inverter is implemented in MATLAB/Simulink to examine the relationship between normal switching operation, fault-induced disturbances, and active fault-tolerant recovery. The simulation framework integrates the power-conversion circuit with modulation, fault injection, diagnostic supervision, and corrective switching. This arrangement allows the inverter response to be assessed under three conditions: healthy operation, operation with a fault and without compensation, and operation with the fault-tolerant controller enabled. Maintaining equivalent source, load, and modulation settings across these conditions provides a consistent basis for evaluating the effect of the control arrangement.

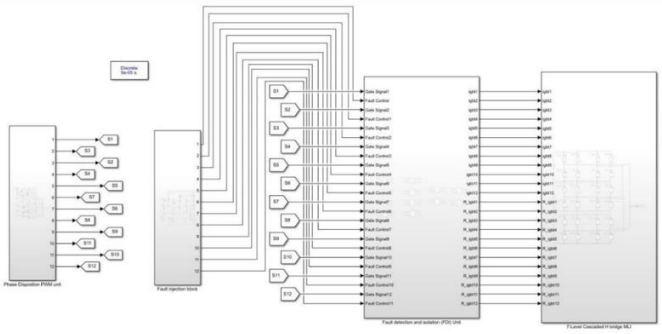


FIGURE 1: MATLAB SIMULINK MODEL OF NINE-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

The power-conversion subsystem uses cascaded H-bridge cells to construct the output voltage from individual cell contributions. In a conventional symmetrical nine-level configuration, four H-bridge cells are supplied by equal isolated DC sources. Each cell can contribute a positive voltage, zero voltage, or negative voltage, depending on its switching state. The series combination of these contributions produces nine possible output-voltage levels. By selecting an appropriate sequence of states, the inverter forms a stepped approximation to a sinusoidal waveform. The modular structure also allows the effect of a fault in one cell to be examined separately from the operation of the remaining cells.

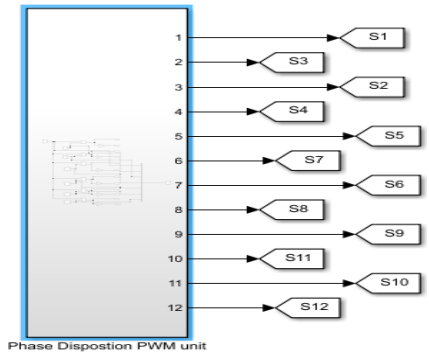


FIGURE 2: PHASE DISPOSITION PWM UNIT

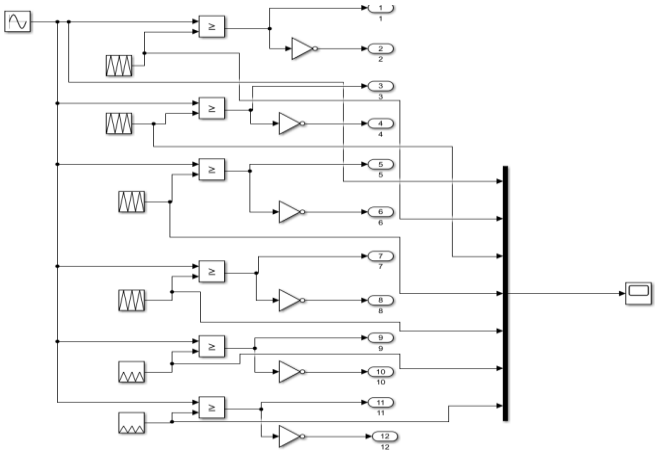


FIGURE 3: INTERNAL BLOCK DIAGRAM OF PHASE DISPOSITION PWM UNIT

The modulation subsystem uses phase-disposition pulse-width modulation to generate the switching commands. A sinusoidal reference is compared with eight triangular carriers arranged in vertically displaced amplitude bands. All carriers have a common frequency and phase, while their vertical positions divide the reference range into the required voltage regions. The comparison results determine the requested output level, and the switching logic translates that request into gating commands for the individual cells. Complementary devices within a bridge leg must be coordinated to prevent an invalid conduction state. The modulation index controls the reference amplitude relative to the carrier arrangement and consequently influences the fundamental output-voltage magnitude.

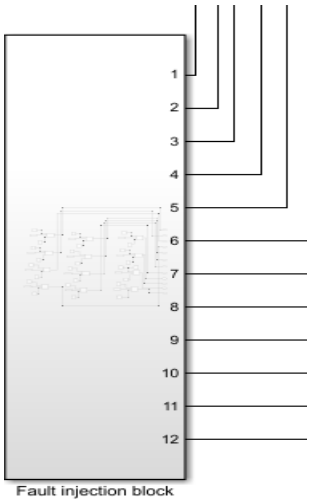


FIGURE 4: FAULT INJECTION BLOCK

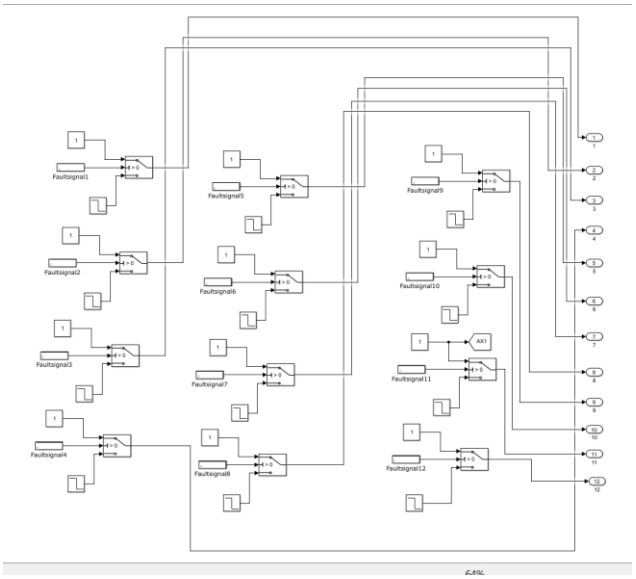


FIGURE 5: INTERNAL BLOCK DIAGRAM OF FAULT INJECTION BLOCK

The healthy operating model establishes the expected relationship between the commanded switching states and the resulting inverter output. Voltage and current measurements provide the signals required for performance assessment and diagnostic supervision. Their interpretation must account for normal switching ripple and any transient associated with startup or a change in operating conditions. A diagnostic unit that responds to every instantaneous deviation would be unsuitable because switching converters naturally produce rapidly varying signals. The implementation therefore requires an explicit distinction between expected switching behaviour and a sustained deviation associated with a fault.

The fault-injection subsystem introduces a controlled abnormality into a selected switching path. Its role is to make the fault occurrence repeatable so that the response with compensation can be compared against the response without compensation. A complete test definition must identify the affected device, the fault type, the injection instant, and whether the fault remains active for the rest of the simulation. These details are particularly important because an open-switch fault and a short-circuit fault produce different conduction conditions and require different protective responses. The supplied material describes the fault-injection framework but does not establish the exact device-level fault cases or their timing.

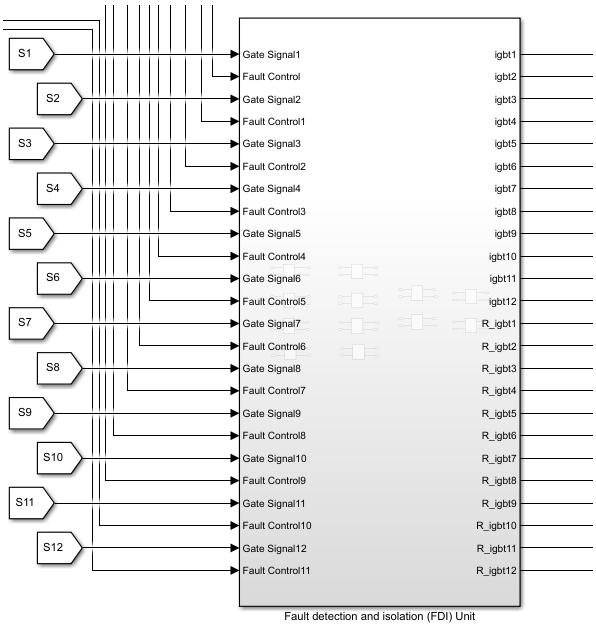


FIGURE 6: FAULT DETECTION AND ISOLATION UNIT

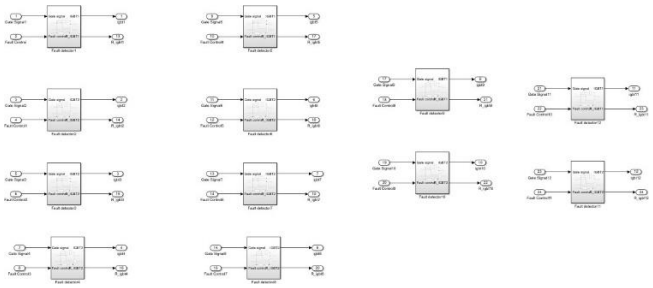


FIGURE 7: INTERNAL BLOCK DIAGRAM OF FAULT DETECTION AND ISOLATION BLOCK

The fault detection and isolation subsystem forms the supervisory part of the controller. It evaluates the monitored signals to determine whether the converter has departed from its expected operating condition. Once an abnormal condition is confirmed, the diagnostic logic must associate it with the affected cell or switch before corrective action is initiated. Changes in output-voltage magnitude, waveform symmetry, and harmonic content can provide useful information, but the implementation must specify how those indicators lead to a particular diagnostic decision. The supplied description does not provide the thresholds, observation windows, or decision rules needed to reproduce this process independently.

Following a diagnostic decision, the controller initiates isolation and recovery. In the intended redundant-switching arrangement, the faulty conduction path is removed from service and an available replacement path assumes its switching function. The timing of this transition is important because the replacement path must be coordinated with the existing gating sequence. Successful recovery depends on whether the redundant circuit can reproduce all the states lost through the fault. If it cannot, continued operation may still be possible with fewer voltage levels or reduced output capability. The implementation should therefore distinguish between maintaining a usable output and fully restoring healthy operation.

The inverter voltage and load current are recorded throughout the simulation to capture the fault transition and subsequent response. The healthy case provides the reference waveform, the uncompensated case reveals the disturbance caused by the fault, and the compensated case shows the effect of corrective switching. Harmonic analysis is then applied to suitable steady-state intervals. Using the same analysis settings across the three cases is essential because changes in the FFT window, harmonic range, or measured signal can otherwise produce misleading differences in total harmonic distortion.

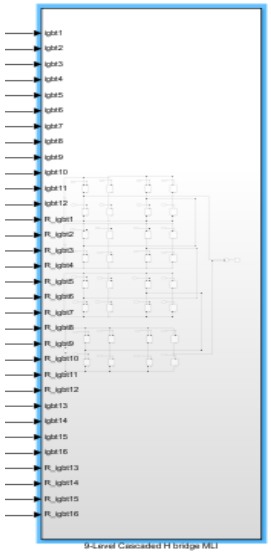


FIGURE 8: 9-LEVEL CASCADE H- BRIDGE MULTI LEVEL INVERTER

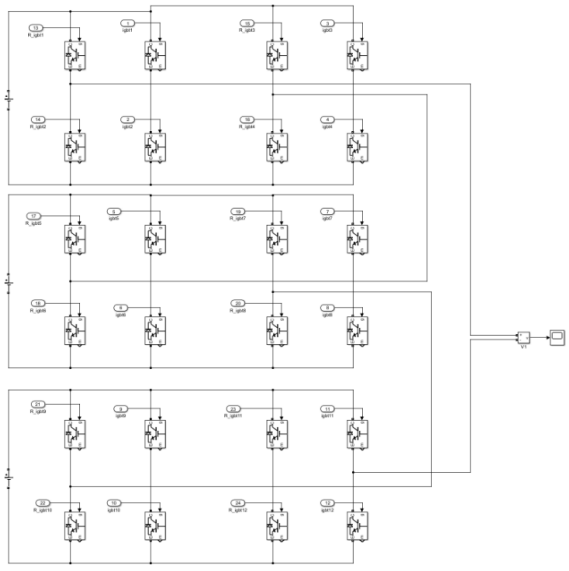


FIGURE 9: INTERNAL BLOCK DIAGRAM OF 9-LEVEL CASCADE H- BRIDGE MULTI LEVEL INVERTER

The supplied material establishes the functional organisation of the MATLAB/Simulink model. However, source voltages, load parameters, carrier frequency, modulation index, solver settings, fault timing, and diagnostic thresholds are not included in the attachment. These parameters should accompany the final implementation description so that the simulation can be reproduced and its results interpreted within a clearly defined operating range.

VI. RESULTS AND DISCUSSION

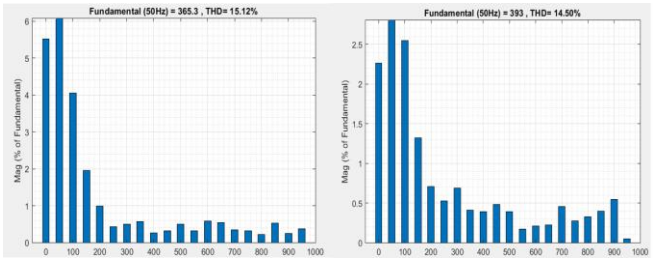


FIGURE 10: DIFFERENT THD WAVE FORMS

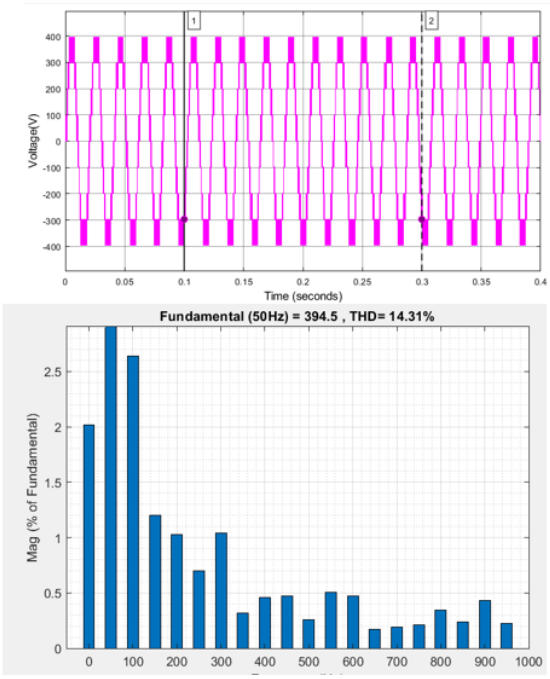


FIGURE 11: WAVE FORMS IN WITHOUT FAULT CONDITION

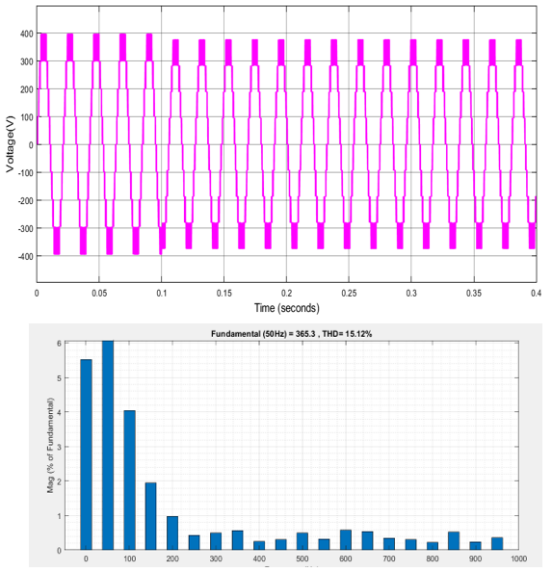


FIGURE 12: WAVEFORMS WITH FAULT CONDITION

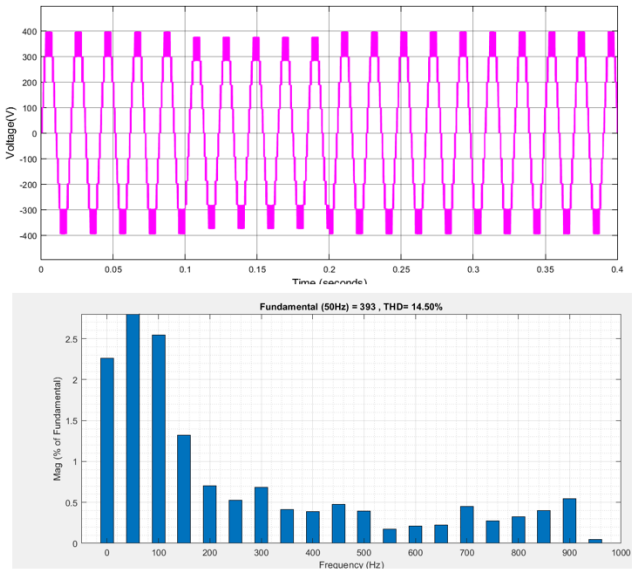


FIGURE 13: WAVE FORMS OF FAULT TOLERANT CONTROL

6.1 Performance Under Healthy Operating Conditions

Healthy operation establishes the reference performance of the inverter before any fault is introduced. Under this condition, the H-bridge cells respond to their assigned switching commands and contribute the voltage states required to construct the multilevel output. The expected response is a repeatable stepped waveform with balanced positive and negative portions. The availability of the intended voltage levels indicates that the cells are participating in voltage synthesis as commanded.

The healthy load-current waveform provides an additional reference for evaluating converter performance. Its shape depends on the connected load, the applied voltage, and any

filtering present in the circuit. For an inductive load, current generally changes more gradually than the switched voltage because the inductance limits its rate of change. Consequently, the current waveform cannot be interpreted solely from the number of voltage levels; it must be considered alongside the load parameters and operating frequency.

The diagnostic subsystem should remain inactive during healthy operation. This requirement is significant because a fault-tolerant controller must avoid unnecessary reconfiguration as well as respond to actual faults. Normal switching ripple, startup transients, and legitimate operating changes should not be misclassified as device failures. The healthy case therefore serves two purposes: establishing baseline power-conversion performance and checking the behaviour of the fault-monitoring logic when corrective action is unnecessary.

The attached narrative describes nominal operation, but the waveform images and numerical measurements are unavailable. It is therefore possible to explain the role of the healthy case, while specific conclusions about voltage regulation, current ripple, harmonic distortion, or false-alarm performance remain unverified.

6.2 Effect of a Fault Without Compensation

The uncompensated fault case examines the direct influence of the failed switching path on the inverter output. When a device cannot perform its intended function, the affected cell may no longer produce every commanded voltage state. The resulting output can contain missing steps, unequal positive and negative contributions, or a reduced fundamental component. The precise disturbance depends on the failed device, the current direction, and the remaining conduction paths.

A fault may become visible only when the switching sequence requests the affected state. This distinction matters when evaluating detection delay. The instant at which the fault is injected and the instant at which its electrical consequences become observable are not necessarily identical. A meaningful timing assessment should therefore consider the commanded switching sequence as well as the recorded fault and detection signals.

Changes in the output voltage influence load current and power delivery. A reduction in the fundamental voltage can reduce the useful power transferred to the load, while waveform asymmetry can introduce an unwanted average component. For an inductive load, the current may initially remain continuous even though the voltage is disturbed. The electrical effect can therefore develop over several switching intervals rather than appear as an immediate interruption of current.

The uncompensated case provides the necessary reference for assessing the benefit of active recovery. Without this comparison, continued operation with the controller enabled would not establish how much performance had been recovered. The supplied text does not provide the corresponding measured waveforms or harmonic values, so the severity of the uncompensated disturbance cannot be quantified from the attachment.

6.3 Fault Detection and Isolation Response

The diagnostic stage connects the observed electrical disturbance to the corrective switching action. Its effectiveness depends on detecting a fault promptly while retaining sufficient confidence in the identified location. A rapid abnormality indication is useful only if it leads to the correct isolation decision. Incorrect localisation could remove a healthy path from service or activate an unsuitable replacement path.

Waveform distortion and voltage deviation can indicate a fault, but they may also change when the load, source voltage, or modulation index changes. The diagnostic rules must therefore be evaluated across the intended operating range. Where several faults produce similar output signatures, additional measurements or switching-state information may be needed to distinguish them.

The supplied description states that the FDI unit identifies the affected component and supports targeted mitigation. However, no diagnostic traces, fault-classification results, or measured detection times are included. The material consequently describes the intended function of the unit rather than demonstrating its accuracy or speed. Those claims require evidence linking the injected fault to the diagnostic output and the subsequent switching command.

6.4 Performance with Fault-Tolerant Control

With the controller enabled, the intended recovery sequence begins after the fault has been detected and localised. The affected path is isolated, and the corrective switching arrangement is activated to restore its contribution to the output. If the redundant hardware reproduces the lost switching states, the inverter can potentially recover the original voltage-level capability. If only part of that function is replaced, the resulting operation must be described in terms of its retained levels and power capability.

The transition to the redundant path is an important part of the assessment. Even when the final waveform resembles healthy operation, the reconfiguration interval may contain a temporary voltage error or current disturbance. The evaluation should therefore consider the entire response from fault occurrence through detection, isolation, replacement-path activation, and settling.

Voltage restoration and current recovery should be examined separately. The controller may restore the commanded voltage states before the load current returns to its reference trajectory. This behaviour is particularly relevant for loads that store energy. A complete recovery assessment should identify when the output returns to a specified tolerance and remains within it, rather than treating the activation command alone as proof of settled operation.

The attached narrative reports continued operation after corrective action. This supports a qualitative description of the recovery objective, but does not establish complete restoration of all nine levels, negligible transients, or a particular recovery time. Those conclusions require the actual compensated waveform and its comparison with the healthy reference.

6.5 Harmonic Distortion Assessment

Total harmonic distortion provides a measure of waveform quality by relating harmonic content to the fundamental component. In this investigation, it is relevant to both the normal multilevel waveform and the distortion introduced by the fault. Its interpretation must identify whether voltage THD or current THD is being evaluated, because the load and any filtering affect these quantities differently.

The healthy, uncompensated, and compensated cases should be analysed using equivalent steady-state windows. Each window should contain an integer number of fundamental periods and exclude the fault transition when the purpose is to assess steady-state distortion. A separate time-domain analysis should examine the transient interval. Combining these two assessments avoids confusing a short recovery disturbance with persistent post-fault harmonic degradation.

Effective compensation would be expected to move the harmonic spectrum towards the healthy reference when it restores the original switching states. Nevertheless, this outcome must be established from the measured spectrum. A reduction in THD alone also does not prove full recovery: the fundamental voltage may remain lower, so its magnitude and delivered power must be assessed alongside distortion.

The attachment contains no readable FFT results, THD values, or analysis settings. It therefore does not support a numerical claim about harmonic reduction or compliance with a power-quality limit. The final discussion should report the measured values and their operating conditions before drawing such conclusions.

6.6 Overall Interpretation and Limitations

The described model provides a structured basis for studying active fault management in a nine-level CHB inverter. Its main strength is the coordinated assessment of normal operation, fault-induced degradation, and corrective switching. This comparison can establish whether the proposed arrangement sustains useful output and how closely its compensated response approaches the healthy reference.

The present evidence remains qualitative. The supplied text outlines the intended behaviour but does not include the circuit details, waveform data, diagnostic signals, or numerical measurements needed to verify recovery performance. Claims of uninterrupted operation, accurate switch localisation, improved efficiency, or increased reliability should therefore be limited to what the completed analysis demonstrates.

A defensible conclusion from the supplied material is that the simulation framework is designed to investigate fault accommodation through coordinated detection, isolation, and reconfiguration. Demonstrating its effectiveness requires quantitative comparisons of detection delay, recovery time, retained fundamental voltage, load-current response, and harmonic distortion. Reliability improvement requires additional analysis beyond a successful fault-recovery simulation, while practical validation requires consideration of device behaviour, protection, sensing, and switching-transition constraints.

VII. CONCLUSION

This study presented a MATLAB/Simulink framework for investigating active fault-tolerant control in a nine-level cascaded H-bridge multilevel inverter. The framework combines phase-disposition pulse-width modulation, controlled fault injection, fault detection and isolation, and corrective switching. Its central purpose is to coordinate fault identification with an appropriate recovery action so that converter operation can be sustained under supported fault conditions.

The assessment considers healthy operation, uncompensated fault operation, and operation with fault-tolerant control enabled. These conditions provide a consistent basis for examining fault-induced waveform degradation and the contribution of the recovery arrangement. Output-voltage characteristics, load-current response, retained voltage levels, harmonic distortion, and recovery timing are the principal measures needed to establish its effectiveness. The available documentation describes the intended recovery behaviour, but does not provide sufficient numerical evidence to quantify improvements in harmonic performance, detection speed, or reliability.

The work provides a foundation for further evaluation of coordinated diagnosis and redundant switching in a nine-level inverter. Future development should establish reproducible diagnostic rules, investigate different fault locations and operating conditions, and account for sensing errors, dead time, and isolation-device behaviour. Hardware

validation and a separate reliability assessment are necessary to determine the practical benefits and operating limits of the proposed arrangement.

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